IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Currently Amended) A method of manufacturing a semiconductor device comprising a first semiconductor chip provided with a first electrode on a first main surface and a second semiconductor chip provided with a second electrode on a second main surface, said method comprising:

a first step of integrating a semiconductor wafer to be a plurality of said first semiconductor chips and a plurality of discrete said second semiconductor chips by arranging said first main surface of each said first semiconductor chip in said semiconductor wafer to be opposed to said second main surface of each said second semiconductor chip and electrically connecting said first electrode on each said first semiconductor chip in said semiconductor wafer and said second electrode on each said second semiconductor chip;

a second step of polishing said second semiconductor chip integrated with said semiconductor wafer from an opposite side of said second main surface so that a thickness of each said second semiconductor chip is made smaller than a thickness of said semiconductor wafer~~, including arranging the distance from said first main surface of each said first semiconductor chip in said semiconductor wafer to a surface of each said second semiconductor chip opposite to said second main surface to be smaller than the distance from said first main surface of each said first semiconductor chip in said semiconductor wafer to the highest position of said bonding wire on said first main surface;~~ and

a third step of separating said semiconductor wafer integrated with said second semiconductor chips into a plurality of discrete said first semiconductor chips, thereby forming a plurality of chip-layered bodies each including a discrete said first semiconductor chip and a discrete said second semiconductor chip integrated with one another;

wherein an area of said first main surface is larger than an area of said second main surface, a third electrode is provided outside a region of said first main surface opposed to said second main surface, and after said third step, said chip-layered bodies are each subjected to the steps of adhering a surface of said first semiconductor chip opposite to said first main surface to a die pad; providing a lead adjacent to said die pad and electrically connecting said lead and said third electrode through a bonding wire; and forming a resin package to encapsulate said first semiconductor chip, said second semiconductor chip and the bonding wire,

said second step comprises the step of arranging the distance from said first main surface of each said first semiconductor chip in said semiconductor wafer to a surface of each said second semiconductor chip opposite to said second main surface to be smaller than the distance from said first main surface of each said first semiconductor chip in said semiconductor wafer to the highest position of said bonding wire on said first main surface.

2. (Original) The method of manufacturing a semiconductor device according to claim 1, wherein

said first step comprises the step of forming a resin layer between said first main surface of each said first semiconductor chip in said semiconductor wafer and said second main surface of each said second semiconductor chip.

3. (Original) The method of manufacturing a semiconductor device according to claim 1, wherein

said second step comprises the step of reducing the thickness of each said second semiconductor chip to at most 1/2 of the thickness of said semiconductor wafer.